(Pages : 2) **8721**

Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, December 2015
(2008 Scheme)
Branch : Electronics & Communication Engineering
08.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Four** marks **each**.

1. Using Dc Morgan's Theorems, find the equivalent to F = ab + ac.
2. Find the minimal POS using k-map P = π (0, 2, 5, 7, 8, 10, 13, 15).
3. Write VHDL programme for a half adder.
4. What are the input and output logic levels of CMOS ?
5. What are the advantages of edge triggered flip flops over level triggered one ?
6. Distinguish between positive and negative logic.
7. Design a monostable multivibrator using 74121 to obtain a pulse of width 100 ms. Draw the circuit diagram.
8. Draw a asynchronous machine model and explain.
9. What are races and cycles that exist in asynchronous machines ?
10. What are the guidelines for making a state assignment ?

P.T.O.

PART – B

Answer **any 2** questions from **each** Module. **Each** question carries **10** marks.

Module – 1

11. Using Quine Mc Cluskey method, simplify
$F = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11, 12)$

12. Design a 2 digit BCD adder using 74LS83.

13. a) Design and implement a 3 bit look ahead carry adder.
    b) What are the differences between static RAM and Dynamic RAM ?

Module – 2

14. a) Explain the operation of a ECL OR/NOR gate.
    b) What are the applications of open collector gates ?

15. Design a counter to count the sequence 3-2-5-7-6-3.

16. a) Draw the circuit of a 5-bit ring counter and explain its working.
    b) What is race-around condition ? How it can be eliminated ?

Module – 3

17. a) Define state variable and excitation variable with example.
    b) Explain the steps for synchronous sequential circuits analysis.

18. Create a shared row state assignment for the following flow table.

Present State	Next State			
	00	01	10	11
a	(a)	b	(a)	b
b	c	(b)	(b)	(b)
c	(c)	d	b	d
d	(d)	(d)	a	(d)

19. a) Explain static hazards, dynamic hazards and essential hazards with examples.
    b) Design a hazard free combinational circuit "
$f = \sum (0, 1, 3, 4, 5, 12, 13)$